1. (Currently Amended) An active pixel sensor circuit comprising:

a photodetector;

an access transistor connected to the photodetector;

an electronically reconfigurable transistor, successively operated as a source follower driver and a feedback amplifier, connected to an output of the access transistor and to a signal output bus; ~~and~~

a reset transistor connected between the access transistor and the ~~amplifier~~ electronically reconfigurable transistor, wherein the reset transistor is reset with a tapered reset signal; and

a first column buffer connected to the electronically reconfigurable transistor and to the reset transistor, the first column buffer comprising:

a first switch transistor connected to the reset transistor; and

a second switch transistor connected to the electronically reconfigurable transistor;

wherein during a reset operation, the first and second switch transistors connect the reset transistor with the electronically reconfigurable transistor to form a feedback path.

2. (Original) The circuit of Claim 1, wherein the transistors are MOSFETs of identical polarity.

3. (Cancelled)

4. (Currently Amended) The circuit of Claim ~~3~~ 2, further comprising a second column buffer connected to the signal output bus.

5. (Original) The circuit of Claim 4, further comprising a row disable transistor connected to the reset transistor.

6. (Original) The circuit of Claim 5, wherein the first column buffer, second column buffer and row disable transistor are connected to a plurality of active pixel sensor circuits.

7. (Previously Presented) The circuit of Claim 6, wherein the electronically reconfigurable transistor operates as a driver of a source follower amplifier when a signal from the photodetector is being read out on a row-by-row basis, and operates as a driver of a reset amplifier when the photodetector is being reset.

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) A CMOS imager array comprising a plurality of pixels, each pixel
comprising:

a photodetector;

an access MOSFET having a source connected to the photodetector;

an amplifier MOSFET having a gate connected to a drain of the access MOSFET, a source connected to a signal bus, and a drain connected to a column buffer;

a reset MOSFET having a source connected to the drain of the access MOSFET, a drain connected to the column buffer, and a gate connected to a tapered reset signal generator; and

a distributed feedback amplifier comprising the amplifier MOSFET, the reset MOSFET and the column buffer to taper reset the photodetector,

wherein the column buffer comprises:

a first switch transistor connected to drain of the reset MOSFET; and

a second switch transistor connected to the drain of the amplifier MOSFET;

wherein during a reset operation, the first and second switch transistors connect the drain of the reset MOSFET with the drain of the amplifier MOSFET to form a feedback path.

11. (Original) The imager array of Claim 10, further comprising a row disable MOSFET having a source connected to the drain of the reset MOSFET and a drain connected to a row disable signal generator.

12. (Original) The imager array of Claim 11, further comprising an access signal generator connected to the gate of the access MOSFET.

13. (Currently Amended) The imager array of Claim 12, further comprising a second column buffer connected to the signal bus.

14. (Original) The imager array of Claim 13, wherein the MOSFETs within each pixel are of identical polarity.

15. (Original) The imager array of Claim 14, wherein the photodetector comprises a substrate diode with the silicide cleared.

16. (Cancelled)

17. (New) An active pixel sensor circuit comprising:

a photodetector;

an access transistor connected to the photodetector;

an amplifier transistor, connected to an output of the access transistor and to a signal output bus;

a reset transistor connected between the access transistor and the amplifier transistor, wherein the reset transistor is reset with a tapered reset signal; and

a first column buffer connected to the amplifier transistor and to the reset transistor, the first column buffer comprising:

a first switch transistor connected to the reset transistor; and

a second switch transistor connected to the amplifier transistor;

wherein during a reset operation, the first and second switch transistors connect the reset transistor with the amplifier transistor to form a feedback path.